UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/636,024	04/19/1996	JACK D. PIPPIN	042390.P1674	2339

7590 06/17/2003

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025

EXAMINER	
BRODA, SAMUEL	
ART UNIT	PAPER NUMBER
2123	10

DATE MAILED: 06/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	08/636,024	PIPPIN, JACK D.	
	Examiner	Art Unit	
	Samuel Broda	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *5/22/98; 2/5/01; 3/22/01; 5/31/02* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *37-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *37-53* is/are allowed.

6)☒ Claim(s) *54-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 March 1995* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *24- 26* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This communication is in response to:

1) Applicant's Amendment sent via facsimile on 22 May 1998 (Paper No. 23); and

2) Applicant's submission of Information Disclosure Statements mailed on:

a) 30 January 2001 (Paper No. 24);

b) 13 March 2001 (Paper No. 25); and

c) 31 May 2002 (Paper No. 26).

In the Amendment, claims 49 and 51 were amended; claims 37-60 are pending.

Information Disclosure Statement

2. Many of the items appearing in the submitted Information Disclosure Statements are references already made of record in this case. Items already of record but appearing in the submitted Information Disclosure Statements have been crossed out.

Request for Declaration of Interference

3. Applicant previously submitted a Request for Declaration of Interference Pursuant to 37 C.F.R. §1.607 (the "Interference Request") in Paper No. 13. Based on the claim interpretations and rejections below, claims 54 and 59 are determined to not be claiming substantially the same invention as claimed in U.S. Patent 5,451,892 to Bailey.

3.1 In Applicant's Interference Request, Applicant proposes Applicant's independent claim 59 as Count 1 and Applicant's independent claim 54 as Count 2.

In Count 1, Applicant states that the limitation:

> means for varying the associated frequency of the clock signal in response to at least one of the first and second signals

(as appearing in Applicant's claim 59) corresponds to the limitation:

> a clock management unit coupled to receive said primary indicator signal and said auxiliary indicator signal, and coupled to said frequency control circuit, wherein said clock management unit is configured to vary said control signal to thereby cause a change in the frequency of said timing signal in response to assertions of said primary indicator signal and said auxiliary indicator signal

as appearing in claim 1 of U.S. Patent 5,451,892.

In Count 2, Applicant states that the limitation:

> d) varying a frequency of the clock signal in response to at least one of the first and second threshold signals

(as appearing in Applicant's claim 54) corresponds to the limitations:

> decreasing a frequency of said internal clock signal if said primary indicator signal is asserted; and
>
> increasing said frequency of said internal clock signal if neither said primary indicator signal nor said auxiliary indicator signal are asserted.

as appearing in claim 18 of U.S. Patent 5,451,892.

3.2 However, Applicant's Specification appears to only provide support for decreasing a clock frequency based on at least one of the first and second threshold signals, whereas the invention of Bailey includes circuitry for decreasing and increasing the clock frequency. See Bailey, column 5 lines 28-61 and column 8 lines 20-32.

3.3 Therefore, claims 54 and 59 are determined to not be claiming substantially the same invention as claimed in U.S. Patent 5,451,892 to Bailey.

Claim Rejections - 35 U.S.C. § 112, First Paragraph

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4.1 Claim 57 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

4.2 Regarding claim 57, this claim adds to step d) of independent claim 54 "the step of increasing the frequency of the clock signal if neither the first threshold signal nor the second

threshold signal are asserted." However, the Specification appears to fail to state any connection between increasing the frequency of the clock signal and the two threshold signals.

The Specification text appears to only mention the increasing of the frequency of the clock signal at pages 5 and 25. At page 5 lines 16-21 the Specification states:

> In a second embodiment of the present invention, the interrupt generated by the programmable thermal sensor is input to external sensor logic. The external sensor logic automatically controls the frequency of the microprocessor. If the temperature of the microprocessor raises, then the clock frequency is decreased. Conversely, if the temperature of the microprocessor drops, then the system clock frequency is increased.

Then at page 25 line 20 through page 26 line 2, the Specification states:

> . . . In addition, the processor unit 705 may set a standard timer circuit such that if a pre-determined amount of time elapses, then the processor unit 705 increases the clock frequency. Increasing the clock frequency permits the processor unit 705 to increase performance when the temperature of the microprocessor has decreased. In addition, to detect further decreases in the microprocessor temperature, the microprogram 740 may lower the threshold temperature and the processor unit may further increase the clock frequency. Therefore, the programmable thermal sensor of the present invention is utilized to control the temperature by increasing and decreasing the microprocessor clock frequency.

The text quoted above suggests two potential methods to raise the clock frequency of the microprocessor as:

(1) using a timer circuit that automatically directs the processor to increase the frequency, and

(2) resetting the threshold value in the microprogram.

However, the Specification does not appear to indicate how either method would actually direct the increasing of the clock frequency, as the remainder of the Specification and the drawings appear directed towards lowering of the clock frequency. In any case, neither of these two potential methods to raise the clock frequency appears connected to the assertion (or lack of assertion) of the threshold signals, as appears in claim 57.

Claim Rejections - 35 U.S.C. § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> . . .
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5.1 Claims 54-56 and 58-60 are rejected under 35 U.S.C. 102(e) as being anticipated by Morikawa et al, U.S. Patent 5,379,230 issued 3 January 1995 with effective filing date of 31 October 1991.

5.2 Regarding claim 54, Morikawa et al teaches a semiconductor integrated circuit including a temperature sensor and hardware and software that monitors the integrated circuit

and reduces power to a load when the integrated circuit exceeds a set of temperature thresholds. See Figs. 3 and 4.

In particular, Morikawa et al teaches a method of controlling the frequency of a clock signal which drives a microprocessor, comprising the steps of:

a) generating a temperature signal within the microprocessor corresponding to a temperature of the microprocessor [sensor 5 on semiconductor chip 1; see Fig. 3];

b) generating a first threshold signal if the temperature signal indicates that the microprocessor temperature exceeds a first threshold temperature [signal generated when threshold temperature T_1 equals 130 degrees Celsius at step 405; see Fig. 4];

c) generating a second threshold signal if the temperature signal indicates that the microprocessor temperature exceeds a second threshold temperature [signal generated when threshold temperature T_1 equals 160 degrees Celsius at step 406; see Fig. 4]; and

d) varying a frequency of the clock signal in response to at least one of the first and second threshold signals [connection of temperature sensor to microprocessor unit MPU 2 so that the temperature sensor places an upper frequency limit of the MPU 2; see column 7 lines 17-24].

Therefore, Morikawa et al anticipates claim 54.

5.3 Regarding claim 55, Morikawa et al teaches programming the threshold levels within programmable registers. See column 3 line 52 through column 4 line 26.

5.4 Regarding claim 56, Morikawa et al teaches reduction of frequency when the temperature sensor oscillates past an upper frequency limit corresponding to a first threshold limit. See column 7 lines 17-24.

5.5 Regarding claim 58, Morikawa et al teaches reduction of frequency (corresponding to setting drivability to 80%) when a threshold temperature T_1 is less than 130 degrees Celsius but greater than 100 degrees Celsius at stop 406 at step 405; see Fig. 4.

5.6 Regarding claims 59-60, system claims 59-60 correspond to method claims 54-55 and are anticipated using the analysis of claim 54-55 above.

Allowable Subject Matter

6. Claims 37-53 are allowed.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure. Reference to Broadwater et al, U.S. Patent 4,970,497 issued 13 November 1990, is cited as teaching the harmful effects of thermal stress on integrated semiconductor chips and using a set of inverters or gates as temperature sensors on a semiconductor chip.

8. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Samuel Broda, whose telephone number is (703) 305-1026. The Examiner can normally be reached on Mondays through Fridays from 8:00 AM – 4:30 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone numbers for this group are:

(703) 746-7238 --- for communications after a Final Rejection has been made;

(703) 746-7239 --- for other official communications; and

(703) 746-7240 --- for non-official or draft communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

SAMUEL BRODA, ESQ.
PRIMARY EXAMINER